Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A ~~Modulator~~ modulator for generating a digital I/Q signal having a plurality of time-slots, the modulator comprising:

a first branch of 0^{th} order with a first pulse-shaping filter for providing a first linearly modulated signal in an I/Q domain;

at least one second branch of higher order with a second pulse-shaping filter for providing a second linearly modulated signal in the I/Q domain;

an adder for adding the first linearly modulated signal and the second linearly modulated signal to approximate a GMSK modulator; and

means for introducing a dip in an envelope of the digital I/Q signal in a guard interval between adjacent time-slots of the plurality of time-slots, ~~wherein~~ the means for introducing the dip in the envelope of the digital I/Q signal in the guard interval between the adjacent time-slots of the plurality of time-slots including means for filling digital zeros into the first pulse-shaping filter and the second pulse-shaping filter~~comprises a digital multiplier for multiplying at least one of the I signal and the Q signal of the I/Q signal with a dip-shaped waveform~~.

2-5. (Canceled)

6. (Currently Amended) The ~~Modulator~~ modulator in accordance with claim 1, ~~wherein the modulator is a GMSK modulator and a~~ further including an 8PSK modulator including said first pulse-shaping filter.

7. (Currently Amended) ~~Signal~~ A signal processing method for generating a digital I/Q signal having a plurality of time-slots, the signal processing method comprising the steps of:

~~(a) modulating the I signal and the Q signal for generating the I/Q signal; and~~

~~(b)~~

under control of a modulator, generating a digital I/Q signal by,

generating a first linearly modulated signal of a 0^{th} order in an I/Q domain using a first pulse-shaping filter;

generating a second linearly modulated signal of a higher order in the I/Q domain using a second pulse-shaping filter in a quadratic branch; and

adding the first linearly modulated signal and the second linearly modulated signal to approximate a GMSK modulator; and

generating ~~introducing~~ a dip in an envelope of the digital I/Q signal in a guard interval between adjacent time-slots of the plurality of time-slots by filling digital zeros into the first pulse-shaping filter and the second pulse-shaping filter~~,~~

~~wherein the introducing includes multiplying at least one of the I signal and the Q signal of the I/Q signal with a dip-shaped waveform~~.

8-11. (Canceled)

12. (New) The modulator of claim 1, wherein the guard interval is formed by a plurality of guard bits, the means for filling digital zeros including means for filling digital zeros into the first pulse-shaping filter and the second pulse-shaping filter during all the guard bits except a first guard bit and a last guard bit.

13. (New) The modulator of claim 1, wherein the first branch includes a first mapper for receiving GMSK bits, a first digital multiplier for multiplying an output of the first mapper by a first complex phasor corresponding to an order to the first branch, a first multiplexer for feeding digital zeros or an output of the first digital multiplier, a first up-sampler for inserting

zeros into an output of the first multiplexer and for providing an output thereof to the first pulse-shaping filter, wherein the second branch includes a finite state machine for receiving the GMSK bits, a second mapper for receiving an output of the finite state machine, a second digital multiplier for multiplying an output of the second mapper by a second complex phasor corresponding to an order to the second branch, a second multiplexer for feeding digital zeros or an output of the second digital multiplier, a second up-sampler for inserting zeros into an output of the second multiplexer and for providing an output thereof to the second pulse-shaping filter.

14. (New) The modulator of claim 6, wherein the guard interval is formed by a plurality of guard bits, the means for filling digital zeros including means for filling digital zeros into the second pulse-shaping filter during each time slot in an 8PSK mode of operation, filling digital zeros into the first pulse-shaping filter and the second pulse-shaping filter during all the guard bits except a first guard bit during a switching from a time slot in a GMSK mode of operation to a time slot in the 8PSK mode, and filling digital zeros into the first pulse-shaping filter and the second pulse-shaping filter during all the guard bits except a last guard bit during a switching from a time slot in the 8PSK mode to a time slot in the GMSK mode.

15. (New) The modulator of claim 6, wherein the first branch includes a first mapper for receiving GMSK bits, a first digital multiplier for multiplying an output of the first mapper by a first complex phasor corresponding to an order to the first branch, a first multiplexer, and a first up-sampler; and wherein the 8PSK modulator includes a serial to parallel converter for receiving a serial data stream, a grey mapper for mapping an output of the serial to parallel converter into a complex signal, a further digital multiplier for multiplying an output of the grey mapper by a further complex phasor, said first multiplexer for feeding digital zeros, the output of the first digital multiplier or an output of the further multiplier, said first up-sampler for inserting zeros into the output of the first multiplexer and for providing an output thereof to said first pulse-shaping filter, and a further multiplexer for selecting the 8PSK modulator or the GMSK modulator.

16. (New) The signal processing method of claim 7, wherein the guard interval is formed by a plurality of guard bits, the filling digital zeros further includes filling digital zeros into the first pulse-shaping filter and the second pulse-shaping filter during all the guard bits except a first guard bit and a last guard bit.

17. (New) A signal processing method, comprising:

under control of a modulator,

generating a digital I/Q signal having a plurality of time-slots by selectively using a GMSK modulation scheme when operating in a GMSK mode of operation and an 8PSK modulation scheme when operating in an 8PSK mode of operation, wherein the GMSK modulation scheme approximates a GMSK modulator to generate the digital I/Q signal by adding a series of at least two linearly modulated signals in an I/Q domain, wherein a first of the at least two linearly modulated signals is a 0^{th} element of the series and is generated using a first pulse-shaping filter and a second of the at least two linearly modulated signals is a higher order element of the series and is generated using a second pulse-shaping filter, and wherein the 8PSK modulation scheme uses a 8PSK modulator to generate the digital I/Q signal, the 8PSK modulator including the first pulse-shaping filter; and

generating a dip in an envelope of the digital I/Q signal in a guard interval between adjacent time-slots of the plurality of time-slots by filling digital zeros into at least one of the first pulse-shaping filter and the second pulse-shaping filter.

18. (New) The signal processing method of claim 17, the guard interval is formed by a plurality of guard bits, and the filling digital zeros further includes filling digital zeros into the second pulse-shaping filter during each time slot in the 8PSK mode of operation, filling digital zeros into the first pulse-shaping filter and the second pulse-shaping filter during all the guard bits except a first guard bit during a switching from a time slot in the GMSK mode of operation to a time slot in the 8PSK mode of operation, and filling digital zeros into the first pulse-shaping filter and the second pulse-shaping filter during all the guard bits except a last

guard bit during a switching from a time slot in the 8PSK mode of operation to a time slot in the GMSK mode of operation.

19. (New) A transmitter, comprising:

a modulator for generating a digital I/Q signal having a plurality of time-slots, the modulator comprising:

a first branch of 0^{th} order with a first pulse-shaping filter for providing a first linearly modulated signal in an I/Q domain;

at least one second branch of higher order with a second pulse-shaping filter for providing a second linearly modulated signal in the I/Q domain;

an adder for adding the first linearly modulated signal and the second linearly modulated signal to approximate a GMSK modulator; and

means for introducing a dip in an envelope of the digital I/Q signal in a guard interval between adjacent time-slots of the plurality of time-slots, the means for introducing the dip in the envelope of the digital I/Q signal in the guard interval between the adjacent time-slots of the plurality of time-slots including means for filling digital zeros into the first pulse-shaping filter and the second pulse-shaping filter.

20. (New) The transmitter of claim 19, wherein the guard interval is formed by a plurality of guard bits, the means for filling digital zeros including means for filling digital zeros into the first pulse-shaping filter and the second pulse-shaping filter during all the guard bits except a first guard bit and a last guard bit.

21. (New) The transmitter of claim 19, wherein the first branch includes a first mapper for receiving GMSK bits, a first digital multiplier for multiplying an output of the first mapper by a first complex phasor corresponding to an order to the first branch, a first multiplexer for feeding digital zeros or an output of the first digital multiplier, a first up-sampler for inserting zeros into an output of the first multiplexer and for providing an output thereof to the first pulse-shaping filter, wherein the second branch includes a finite state machine for

receiving the GMSK bits, a second mapper for receiving an output of the finite state machine, a second digital multiplier for multiplying an output of the second mapper by a second complex phasor corresponding to an order to the second branch, a second multiplexer for feeding digital zeros or an output of the second digital multiplier, a second up-sampler for inserting zeros into an output of the second multiplexer and for providing an output thereof to the second pulse-shaping filter.

22. (New) The transmitter of claim 19, wherein the modulator further including an 8PSK modulator including said first pulse-shaping filter.

23. (New) The transmitter of claim 22, wherein the guard interval is formed by a plurality of guard bits, the means for filling digital zeros including means for filling digital zeros into the second pulse-shaping filter during each time slot in an 8PSK mode of operation, filling digital zeros into the first pulse-shaping filter and the second pulse-shaping filter during all the guard bits except a first guard bit during a switching from a time slot in a GMSK mode of operation to a time slot in the 8PSK mode, and filling digital zeros into the first pulse-shaping filter and the second pulse-shaping filter during all the guard bits except a last guard bit during a switching from a time slot in the 8PSK mode to a time slot in the GMSK mode.

24. (New) The transmitter of claim 22, wherein the first branch includes a first mapper for receiving GMSK bits, a first digital multiplier for multiplying an output of the first mapper by a first complex phasor corresponding to an order to the first branch, a first multiplexer, and a first up-sampler; and wherein the 8PSK modulator includes a serial to parallel converter for receiving a serial data stream, a grey mapper for mapping an output of the serial to parallel converter into a complex signal, a further digital multiplier for multiplying an output of the grey mapper by a further complex phasor, said first multiplexer for feeding digital zeros, the output of the first digital multiplier or an output of the further multiplier, said first up-sampler for inserting zeros into the output of the first multiplexer and for providing an output thereof to said

first pulse-shaping filter, and a further multiplexer for selecting the 8PSK modulator or the GMSK modulator.